REMARKS

I. Introduction

Claims 35-75 are pending in the application.

Applicants note with appreciation that the Examiner has allowed claims 35-51 and has indicated that claims 53, 56 and 63 contain subject matter allowable over the prior art.

Claims 53, 56, and 63 are objected to as being dependent on a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 52, 54-55, 57-62 and 64-75 are rejected under 35 U.S.C. § 102(e).

Reconsideration of this application in light of the following remarks is respectfully requested.

II. The Rejections Based on 35 U.S.C. § 102(e)

The Examiner rejected claims 52, 54-55, 57-62 and 64-75 under 35 U.S.C. § 102(e), as being anticipated by Pierce et al. U.S. Patent 5,581,199 (hereinafter "Pierce"). Applicants respectfully traverse.

The Examiner rejected the above-identified claims contending that Pierce teaches applicants' invention substantially as claimed, including a plurality of

programmable logic elements to select between a first logic standard and a second logic standard wherein the second logic standard is a differential logic standard. Applicants respectfully disagree.

Claims 52, 62, 71 and 74 and are directed towards methods and apparatus that allow an electronic device to select a logic standard from at least one of two available logic standards (one being differential) and operate at the selected standard. One advantage of this configuration is that it provides an I/O architecture that can easily adapt to external environments that operate different logic levels. One deficiency of prior art electronic devices is that their I/O circuitry is typically compatible with only one type of logic standard. Thus, if an end user needs to connect to external circuitry employing standard TTL logic (Transistor-to-Transistor Logic), an electronic device that can provide and receive the appropriate drive signals is needed. However, simply changing the external environment to one that operates at a different logic standard, such as an open-drain CMOS, may require a different electronic device, although the basic device is substantially the same. Applicants' invention solves this problem by providing I/O devices and methods that allow the user to programmably select any one of several logic

standards, so that a single electronic device is adaptable and may be used with external circuitry that operates at different logic levels.

In contrast, Pierce fails to show or suggest this feature anywhere. The Examiner has suggested that Pierce shows circuitry capable of operating at first and second logic standards in FIG. 16 and at column 19, lines 14-31 (Office Action at page 3). This is simply not the case. Register 181 is merely an RS flip-flop that acts as a latch. It is well known in the art that discrete flip-flops are only capable of operating at a single logic standard (although Q and QL may change between a logic high and a logic low level within that one logic standard). Logic gates 178 and 180 merely feed the set and reset inputs of RS flip-flop 181.

The Examiner, however, has suggested that the asynchronous and synchronous data transfer protocols mentioned in Pierce constitute operation with first and second logic standards as specified in the claims (Office Action, Page 3). Applicants disagree. The asynchronous and synchronous data transfer protocols mentioned in Pierce relate to methods of data transfer with respect to a particular clock signal. Generally speaking, if two components that exchange data share the same clock signal, the data transfer is considered

synchronous, if the same clock is not used and the clocks are out of phase, the data transfer is asynchronous. Regardless of whether data is transferred in a synchronous or asynchronous fashion, the components shown in Pierce are only capable of operating at a single logic standard (*i.e.*, voltage or power level).

Applicants respectfully submit that the logic standards specified in the claims at issue relate to different voltage and power levels required for discrete components (such as transistors) to properly operate in compliance with a logic standard and are not dependent on clock signals to ensure proper data transfer. For example, a device that operates a with transistor-to-transistor logic standard (TTL, a 0-5 volt logic standard) will not be able to reliably operate using signals operating at a High-Speed Transistor Logic standard (HSTL, a .05 volt logic standard) due to the significant difference in the voltage levels required to generate logic high and logic low signals. Applicants' claimed invention solves this problem by providing I/O circuitry that can programmably switch between various logic standards (*i.e.*, power, voltage, or speed levels) to accommodate different modes of operation. Nowhere in Pierce are I/O circuits shown that can switch between multiple logic

standards as specified in applicants' claims. Accordingly, claims 52, 62, 71 and 74 and those that depend therefrom are allowable.

Moreover, the Examiner contends that the logic low and logic high signals generated by register 181 constitute "differential signals" because the signals are "different" from one another. Applicant respectfully submits that this meaning is inconsistent with the generally accepted meaning in the industry, in which differential signals are understood to mean signals that are generated by taking the difference of two signals and optionally amplifying that difference. Applicants' invention employs a differential amplifier to obtain this type of differential signal (col. 6, lines 36-60). Nowhere in Pierce is this feature shown or suggested. Accordingly, claims 52, 62, 71 and 74 and those that depend therefrom are allowable.

III. Conclusion

The foregoing demonstrates that claims 52, 54-55, 57-62 and 64-75 are allowable. Thus, this application is in

condition for allowance. Reconsideration and allowance are therefore respectfully requested.

Respectfully submitted,

Michael E. Shanahan
Registration Number 43,914
Attorney for Applicants
and Assignee
Customer Number 1473
c/o Fish & Neave
1251 Avenue of the Americas
New York, NY 10020-1104
Tel.: (212)-596-9025

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